**Name – De Silva APC**

**Index – 210098R**

**Group – In21 CSE**

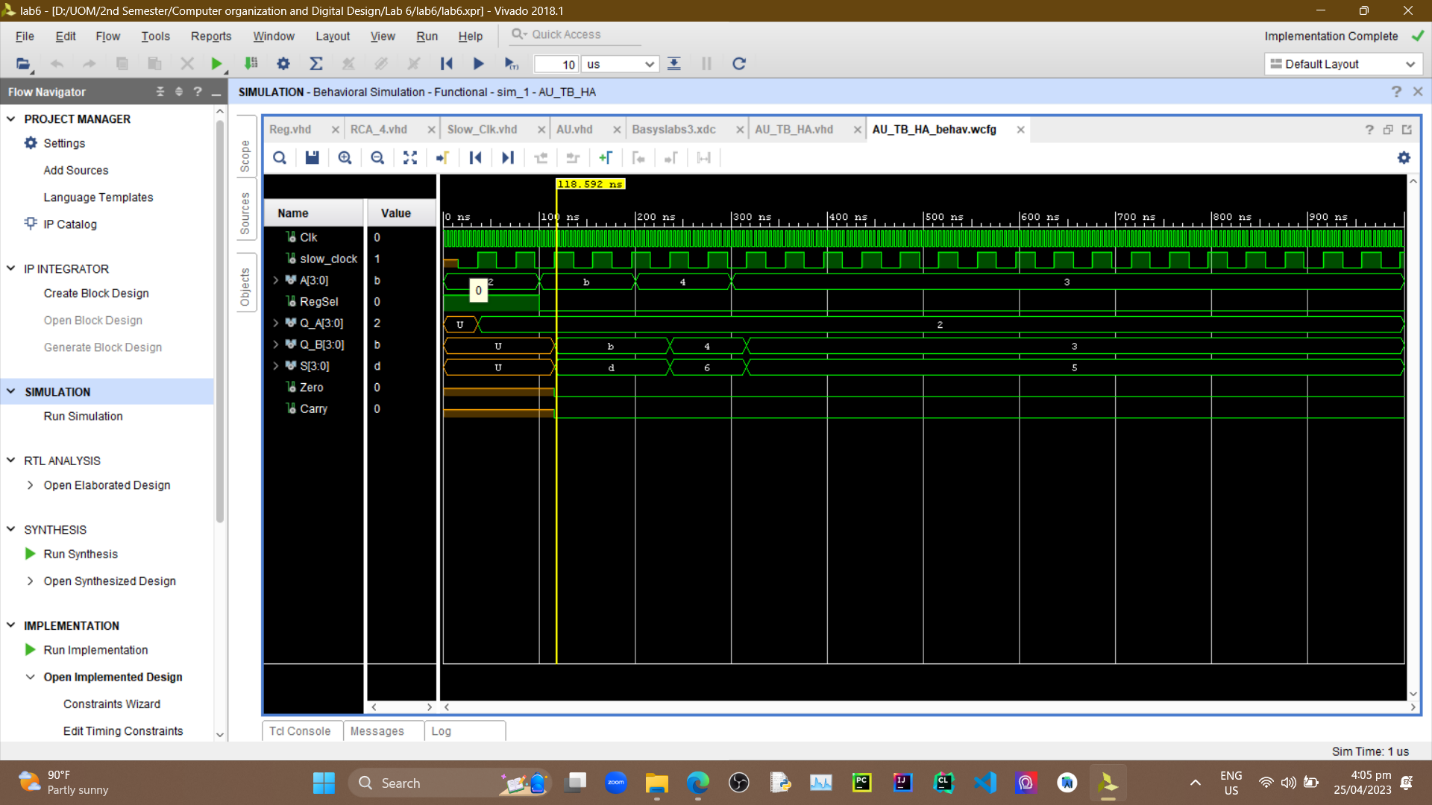
**Assigned Lab Task –**

Main task was to design and develop an (4-bit) Arithmetic unit and then testing it via simulation. The arithmetic unit is deigned to be capable of adding to numbers stored in two registers. This task had the use of the components been designed and developed in previous lab sessions after importing them.

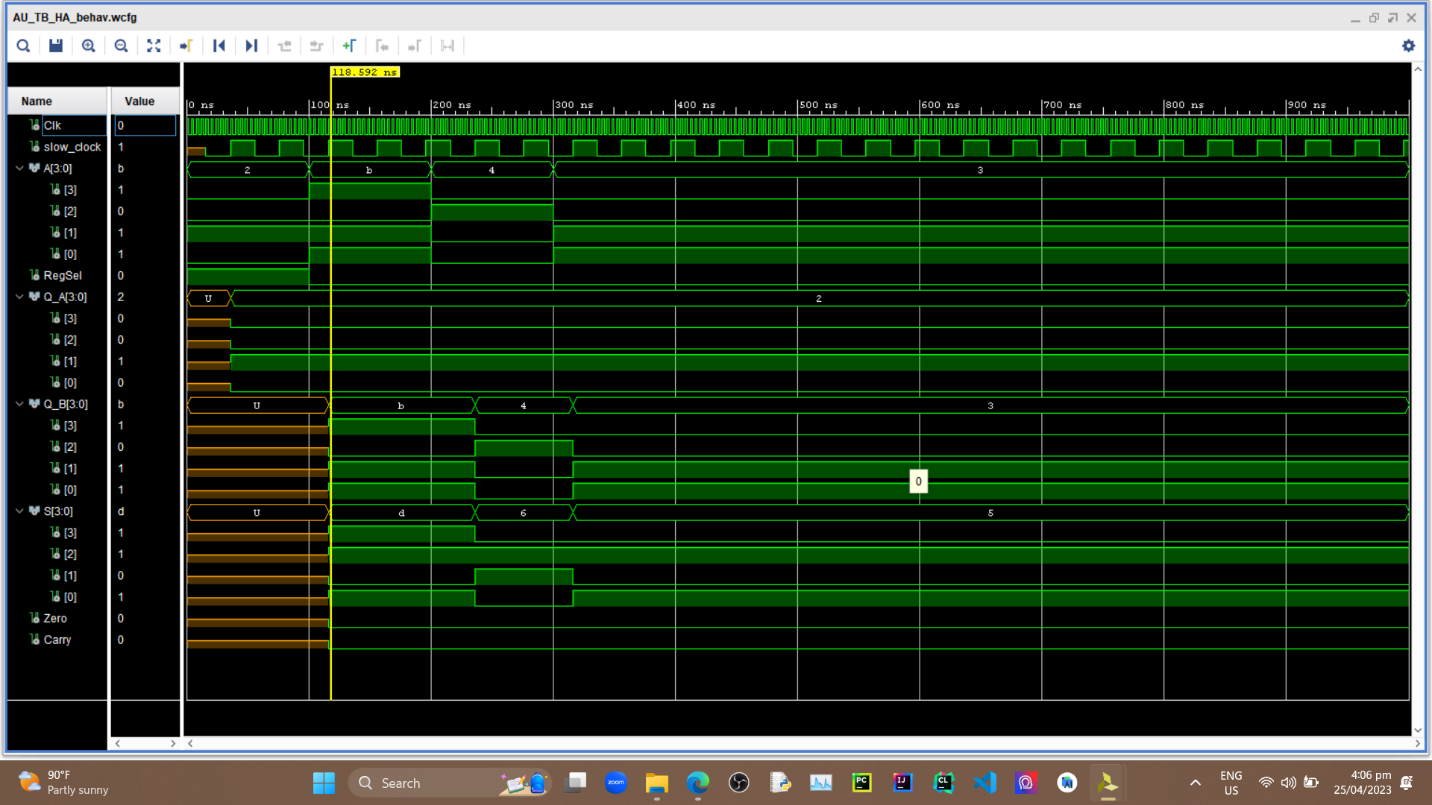
**Conclusions –**

A basic functionality of an Arithmetic logic unit which supports 4 bits. Use of components that already been developed and designed in a larger scale project as modules.

**Screenshots of the simulation(Extended and Archieved) –**

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**(Extended) -**

****

**All VHDL Codes –**

***AU\_TB\_HA.vhd***

*----------------------------------------------------------------------------------*

*-- Company:*

*-- Engineer:*

*--*

*-- Create Date: 04/25/2023 03:17:04 PM*

*-- Design Name:*

*-- Module Name: AU\_TB\_HA - Behavioral*

*-- Project Name:*

*-- Target Devices:*

*-- Tool Versions:*

*-- Description:*

*--*

*-- Dependencies:*

*--*

*-- Revision:*

*-- Revision 0.01 - File Created*

*-- Additional Comments:*

*--*

*----------------------------------------------------------------------------------*

*library IEEE;*

*use IEEE.STD\_LOGIC\_1164.ALL;*

*-- Uncomment the following library declaration if using*

*-- arithmetic functions with Signed or Unsigned values*

*--use IEEE.NUMERIC\_STD.ALL;*

*-- Uncomment the following library declaration if instantiating*

*-- any Xilinx leaf cells in this code.*

*--library UNISIM;*

*--use UNISIM.VComponents.all;*

*entity AU\_TB\_HA is*

*-- Port ( );*

*end AU\_TB\_HA;*

*architecture Behavioral of AU\_TB\_HA is*

*component AU*

*Port ( A : in STD\_LOGIC\_VECTOR (3 downto 0);*

*RegSel : in STD\_LOGIC;*

*Clk : in STD\_LOGIC;*

*S : out STD\_LOGIC\_VECTOR (3 downto 0);*

*Zero : out STD\_LOGIC;*

*Carry : out STD\_LOGIC);*

*end component;*

*signal A,S : STD\_LOGIC\_VECTOR (3 downto 0) :="0000" ;*

*signal RegSel,Clk,Zero,Carry : STD\_LOGIC := '0';*

*begin*

*UUT : AU*

*PORT MAP(*

*A => A,*

*S =>S,*

*Regsel => Regsel,*

*Clk => Clk,*

*Zero => Zero,*

*Carry =>Carry*

*);*

*process*

*begin*

*Clk <= not(Clk);*

*wait for 2ns;*

*end process;*

*process*

*begin*

*A<= "0010";*

*RegSel <= '1';*

*wait for 100ns;*

*RegSel <= '0';*

*A<= "1011";*

*wait for 100ns;*

*A <= "0100";*

*wait for 100ns;*

*A <= "0011";*

*wait;*

*end process;*

*end Behavioral;*

***AU.vhd***

*----------------------------------------------------------------------------------*

*-- Company:*

*-- Engineer:*

*--*

*-- Create Date: 04/25/2023 02:16:58 PM*

*-- Design Name:*

*-- Module Name: AU - Behavioral*

*-- Project Name:*

*-- Target Devices:*

*-- Tool Versions:*

*-- Description:*

*--*

*-- Dependencies:*

*--*

*-- Revision:*

*-- Revision 0.01 - File Created*

*-- Additional Comments:*

*--*

*----------------------------------------------------------------------------------*

*library IEEE;*

*use IEEE.STD\_LOGIC\_1164.ALL;*

*-- Uncomment the following library declaration if using*

*-- arithmetic functions with Signed or Unsigned values*

*--use IEEE.NUMERIC\_STD.ALL;*

*-- Uncomment the following library declaration if instantiating*

*-- any Xilinx leaf cells in this code.*

*--library UNISIM;*

*--use UNISIM.VComponents.all;*

*entity AU is*

*Port ( A : in STD\_LOGIC\_VECTOR (3 downto 0);*

*RegSel : in STD\_LOGIC;*

*Clk : in STD\_LOGIC;*

*S : out STD\_LOGIC\_VECTOR (3 downto 0);*

*Zero : out STD\_LOGIC;*

*Carry : out STD\_LOGIC);*

*end AU;*

*architecture Behavioral of AU is*

*component Slow\_Clk*

*Port ( Clk\_in : in STD\_LOGIC;*

*Clk\_out : out STD\_LOGIC);*

*end component;*

*component RCA\_4*

*Port ( A0 : in STD\_LOGIC;*

*A1 : in STD\_LOGIC;*

*A2 : in STD\_LOGIC;*

*A3 : in STD\_LOGIC;*

*B0 : in STD\_LOGIC;*

*B1 : in STD\_LOGIC;*

*B2 : in STD\_LOGIC;*

*B3 : in STD\_LOGIC;*

*C\_in : in STD\_LOGIC;*

*S0 : out STD\_LOGIC;*

*S1 : out STD\_LOGIC;*

*S2 : out STD\_LOGIC;*

*S3 : out STD\_LOGIC;*

*C\_out : out STD\_LOGIC);*

*end component;*

*component Reg*

*Port ( D : in STD\_LOGIC\_VECTOR (3 downto 0);*

*En : in STD\_LOGIC;*

*Clk : in STD\_LOGIC;*

*Q : out STD\_LOGIC\_VECTOR (3 downto 0));*

*end component;*

*signal slow\_clock : STD\_LOGIC;*

*signal En\_A,En\_B,C\_out : STD\_LOGIC;*

*signal Q\_A, Q\_B,S\_RCA : STD\_LOGIC\_VECTOR (3 downto 0);*

*begin*

*Slow\_Clk\_0 : Slow\_Clk*

*PORT MAP(*

*Clk\_in => Clk,*

*Clk\_out => slow\_clock*

*);*

*Reg\_A : Reg*

*PORT MAP(*

*D=>A,*

*En=>En\_A,*

*Clk=>slow\_clock,*

*Q =>Q\_A*

*);*

*Reg\_B : Reg*

*PORT MAP(*

*D=>A,*

*En=>En\_B,*

*Clk=>slow\_clock,*

*Q =>Q\_B*

*);*

*RCA\_4\_0 : RCA\_4*

*PORT MAP(*

*A0=>Q\_A(0),*

*A1=>Q\_A(1),*

*A2=>Q\_A(2),*

*A3=>Q\_A(3),*

*B0=>Q\_B(0),*

*B1=>Q\_B(1),*

*B2=>Q\_B(2),*

*B3=>Q\_B(3),*

*C\_in=>'0',*

*S0=>S\_RCA(0),*

*S1=>S\_RCA(1),*

*S2=>S\_RCA(2),*

*S3=>S\_RCA(3),*

*C\_out=>C\_out*

*);*

*Carry <= C\_out;*

*S <= S\_RCA;*

*Zero <= not(S\_RCA(0)) and not(S\_RCA(1)) and not(S\_RCA(2)) and not(S\_RCA(3) and not(C\_out));*

*EN\_A <= Regsel;*

*En\_B <= Not(Regsel);*

*end Behavioral;*

***Slow\_Clk.vhd***

*----------------------------------------------------------------------------------*

*-- Company:*

*-- Engineer:*

*--*

*-- Create Date: 04/08/2023 07:25:00 PM*

*-- Design Name:*

*-- Module Name: Slow\_Clk - Behavioral*

*-- Project Name:*

*-- Target Devices:*

*-- Tool Versions:*

*-- Description:*

*--*

*-- Dependencies:*

*--*

*-- Revision:*

*-- Revision 0.01 - File Created*

*-- Additional Comments:*

*--*

*----------------------------------------------------------------------------------*

*library IEEE;*

*use IEEE.STD\_LOGIC\_1164.ALL;*

*-- Uncomment the following library declaration if using*

*-- arithmetic functions with Signed or Unsigned values*

*--use IEEE.NUMERIC\_STD.ALL;*

*-- Uncomment the following library declaration if instantiating*

*-- any Xilinx leaf cells in this code.*

*--library UNISIM;*

*--use UNISIM.VComponents.all;*

*entity Slow\_Clk is*

*Port ( Clk\_in : in STD\_LOGIC;*

*Clk\_out : out STD\_LOGIC);*

*end Slow\_Clk;*

*architecture Behavioral of Slow\_Clk is*

*signal count : integer := 1;*

*signal clk\_status : std\_logic := '0';*

*begin*

*process (Clk\_in) begin*

*if(rising\_edge(Clk\_in)) then*

*count <= count+1;*

*if(count = 5)then -- Counting frequency scaler(Reduced to 5 to simulation purposes.IF not 5M.)*

*clk\_status <= not clk\_status;*

*Clk\_out <= clk\_status;*

*count<=1;*

*end if;*

*end if;*

*end process;*

*end Behavioral;*

***RCA\_4.vhd***

*----------------------------------------------------------------------------------*

*-- Company:*

*-- Engineer:*

*--*

*-- Create Date: 03/18/2023 11:27:04 AM*

*-- Design Name:*

*-- Module Name: RCA\_4 - Behavioral*

*-- Project Name:*

*-- Target Devices:*

*-- Tool Versions:*

*-- Description:*

*--*

*-- Dependencies:*

*--*

*-- Revision:*

*-- Revision 0.01 - File Created*

*-- Additional Comments:*

*--*

*----------------------------------------------------------------------------------*

*library IEEE;*

*use IEEE.STD\_LOGIC\_1164.ALL;*

*-- Uncomment the following library declaration if using*

*-- arithmetic functions with Signed or Unsigned values*

*--use IEEE.NUMERIC\_STD.ALL;*

*-- Uncomment the following library declaration if instantiating*

*-- any Xilinx leaf cells in this code.*

*--library UNISIM;*

*--use UNISIM.VComponents.all;*

*entity RCA\_4 is*

*Port ( A0 : in STD\_LOGIC;*

*A1 : in STD\_LOGIC;*

*A2 : in STD\_LOGIC;*

*A3 : in STD\_LOGIC;*

*B0 : in STD\_LOGIC;*

*B1 : in STD\_LOGIC;*

*B2 : in STD\_LOGIC;*

*B3 : in STD\_LOGIC;*

*C\_in : in STD\_LOGIC;*

*S0 : out STD\_LOGIC;*

*S1 : out STD\_LOGIC;*

*S2 : out STD\_LOGIC;*

*S3 : out STD\_LOGIC;*

*C\_out : out STD\_LOGIC);*

*end RCA\_4;*

*architecture Behavioral of RCA\_4 is*

*component FA*

*port(*

*A: in std\_logic;*

*B: in std\_logic;*

*C\_in : in std\_logic;*

*S: out std\_logic;*

*C\_out : out std\_logic);*

*end component;*

*SIGNAL FA0\_S, FA0\_C , FA1\_S,FA1\_C, FA2\_S, FA2\_C, FA3\_S, FA3\_C*

*: std\_logic;*

*begin*

*FA\_0 : FA*

*port map (*

*A => A0,*

*B => B0,*

*C\_in => '0',*

*S=> S0,*

*C\_out => FA0\_C);*

*FA\_1 : FA*

*port map (*

*A => A1,*

*B => B1,*

*C\_in => FA0\_C,*

*S=> S1,*

*C\_out => FA1\_C);*

*FA\_2 : FA*

*port map (*

*A => A2,*

*B => B2,*

*C\_in => FA1\_C,*

*S=> S2,*

*C\_out => FA2\_C);*

*FA\_3 : FA*

*port map (*

*A => A3,*

*B => B3,*

*C\_in => FA2\_C,*

*S=> S3,*

*C\_out => C\_out);*

*end Behavioral;*

***Reg.vhd***

*----------------------------------------------------------------------------------*

*-- Company:*

*-- Engineer:*

*--*

*-- Create Date: 04/25/2023 02:01:44 PM*

*-- Design Name:*

*-- Module Name: Reg - Behavioral*

*-- Project Name:*

*-- Target Devices:*

*-- Tool Versions:*

*-- Description:*

*--*

*-- Dependencies:*

*--*

*-- Revision:*

*-- Revision 0.01 - File Created*

*-- Additional Comments:*

*--*

*----------------------------------------------------------------------------------*

*library IEEE;*

*use IEEE.STD\_LOGIC\_1164.ALL;*

*-- Uncomment the following library declaration if using*

*-- arithmetic functions with Signed or Unsigned values*

*--use IEEE.NUMERIC\_STD.ALL;*

*-- Uncomment the following library declaration if instantiating*

*-- any Xilinx leaf cells in this code.*

*--library UNISIM;*

*--use UNISIM.VComponents.all;*

*entity Reg is*

*Port ( D : in STD\_LOGIC\_VECTOR (3 downto 0);*

*En : in STD\_LOGIC;*

*Clk : in STD\_LOGIC;*

*Q : out STD\_LOGIC\_VECTOR (3 downto 0));*

*end Reg;*

*architecture Behavioral of Reg is*

*begin*

*process (Clk) begin*

*if (rising\_edge(Clk)) then -- respond when clock rises*

*if En = '1' then -- Enable should be set*

*Q <= D;*

*end if;*

*end if;*

*end process;*

*end Behavioral;*

**THE END OF THE REPORT**